ABSTRACT

[Solution of the Problem According to the Invention] The reduction of the junction electric field intensity in the semiconductor regions for the sources and drains of the field effects transistors.

[Method for Solving the Problem] A structure is provided where the gate electrodes 9 of the MIS•FETQs for memory cell selection of a DRAM are buried within the trenches 7a and 7b created in the semiconductor substrate 1. The bottom corners within the trench 7b are rounded so as to have a radius of curvature in accordance with the sub-threshold coefficient of the MIS•FETQs for memory cell selection. In addition, the gate insulating film 8 within the trench 7b is made to have a laminated structure of a thermal oxide film and a CVD film.

[Selected Drawing] Fig. 28